RESEARCH ARTICLE OPEN ACCESS

A Novel Design of Low Power High Speed Carry Select Adder

U. Sandhya, T. Lakshmi Bhavani, D. Arun kumar, B. Krishna

Abstract
Carry Select Adder (CSLA) is one of the fastest adders used in many computational systems to perform fast arithmetic operations. It performs n-bit addition and provides a sum of n+1 bit. The structure of CSLA gives the future scope of reducing the area and power consumption which are needed for the rapidly growing mobile industry. The modified 64-Bit CSLA architecture has developed using Binary to Excess-1 converter(BEC).This paper proposes an efficient method of replacing RCA in regular proposal with BEC in modified proposal.
Index Terms —Binary To Excess Converter (BEC), Carry Ripple Adder (CRA), Multiplexer (MUX).

I. INTRODUCTION

Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 8-bit, 16-bit, 32-bit, 64-bit CSLA architecture have been developed and compared with the regular CSLA architecture. The proposed design has reduced area and power as compared with the regular CSLA with only a slight increase in the delay.

This work evaluates the performance of the proposed designs in terms of delay, area, power, and their products by hand with logical effort and through custom design and layout. The carry-select adder generally consists of two adders. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known.

II. LITERATURE SURVEY

O.J.BEDRIJ (1971) [1] proposed that the propagation delay can be made overcome by independently generating multiple carries and using these carries to generate simultaneously by generating sums.RAM KUMAR, KITTUR AND KANNAN [2] proposed that a BEC to reduce the maximum delay of carry propagation in final stage of carry save adder. T.Y.CEIANG and M.J.HSIAO [3] proposed the implementation of low power and area efficient carry select adder using D-Latch instead of BEC.Y.KIM and L.S.KIM [4] proposed BEC technique which is a simple and gate level efficient modification to significantly reduce the area and power of SQRT CSLA. The proposed model uses BEC instead of RCA which is used in regular CSLA.

III. RIPPLE CARRY ADDER (RCA)

Ripple carry adder is logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a C_{in}, which is the C_{out} of the previous adder. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder. The sum and the output carry of any stage cannot be produced until the carry input occurs which causes a time delay in the addition process. The carry propagation delay for each full adder is a time from the application of the input carry until the output carry occurs.

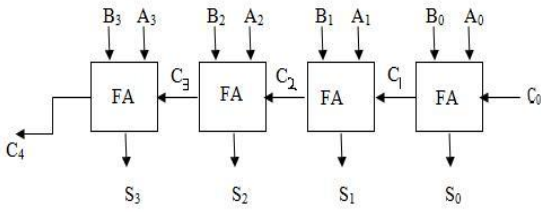

Figure-1: 4-Bit RIPPLE CARRY ADDER

Operation: Full adder1 cannot produce a potential output carry until an input carry is applied. Full adder2 cannot produce a potential output carry until FA1 produces an output carry and so on… The input carry to the least significant stage has to ripple through all the adders before a final sum is produced. The total delay can vary, depending upon the carry bit produced by each FA. If two numbers are added such that no carry occurs between stages, then worst case addition time should be assumed.(The delay through all the FA stages is called **"worst time delay"**)

IV. BINARY TO EXCESS CONVERTER(BEC)

To reduce the area and power consumption Binary Excess-1 converter instead of RCA with Cin = 1. This is the main concept of the paper, so as to reduce dealy compared to regular SQRT CSLA. To replace the n-bit RCA, an n+1 bit BEC is required.The Boolean expressions of the 4-bit BEC is listed as

X0 = ~B0
X1 = B0 ^ B1
X2 = B2 ^ (B0 & B1)
X3 = B3 ^ (B0 & B1 & B2)

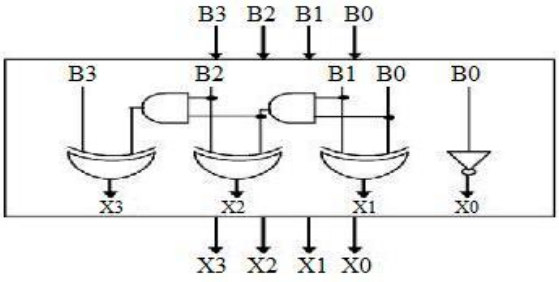

Figure-2: 4-bit Binary to Excess-1 Converter

Binary Logic B0 B1 B2 B3	Excess-1 Logic E0 E1 E2 E3
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

Table-1: Truth Table of 4-Bit BEC

V. MULTIPLEXER (MUX)

One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal cin.

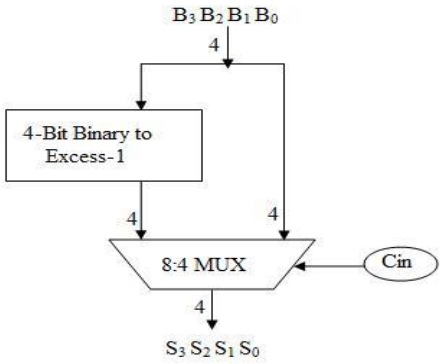

Figure-3: 4-bit Binary to Excess-1 logic with 8:4 multiplexer

VI. ARCHITECTURE OF REGULAR 64-BIT SQRT CSLA:

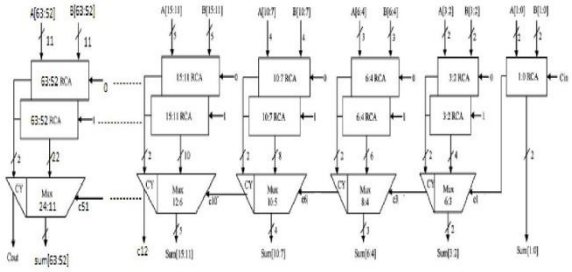

Figure-4: Regular 64-Bit CSLA

A 16-bit carry select adder can be developed in two different sizes namely uniform block size and variable block size. Similarly a 32, 64 and 128-bit can also be developed in two modes of different block sizes. Ripple-carry adders are the simplest and most compact full adders, but their performance is limited by a carry that must propagate from the least-significant bit to the most-significant bit. The various 16, 32, 64 and 128-bit CSLA can also be developed by using ripple carry adders. The speed of a carry-select adder can be improved upto 40% to 90%, by performing the additions in parallel, and reducing the maximum carry delay.Fig 4 shows the Regular structure of 64-bit SQRT CSLA. It includes many ripple carry adders of variable sizes which are divided into groups. Group 0 contains 2-bit RCA which contains only one ripple carry adder which adds the input bits and the input carry and results to sum [1:0] and the carry out. The carry out of the Group 0 which acts as the selection input to mux which is in group 1, selects the result from the corresponding RCA (Cin=0) or RCA (Cin=1). Similarly the remaining groups will be selected depending on the Cout from the previous groups.

In Regular CSLA, there is only one RCA to perform the addition of the least significant bits [1:0].

The remaining bits (other than LSBs), the addition is performed by using two RCAs corresponding to the one assuming a carry-in of 0, the other a carry-in of 1 within a group. In a group, there are two RCAs that receives the same data inputs but different Cin. The upper adder has a carry-in of 0, the lower adder a carry-in of 1. The actual Cin from the preceding sector selects one of the two RCAs. That is, as shown in the Fig.4, if the carry-in is 0, the sum and carry-out of the upper RCA is selected, and if the carry-in is 1, the sum and carry-out of the lower RCA is selected.For this Regular CSLA architecture, the implementation code, for the Full Adders and Multiplexers of different sizes (6:3, 8:4, 10:5 up to 24:11) were designed initially. The regular 64-bit, 128-bit CSLA were implemented by calling the ripple carry adders and all multiplexers.

VII. ARCHITECTURE OF MODIFIED 64-BIT SQRT CSLA

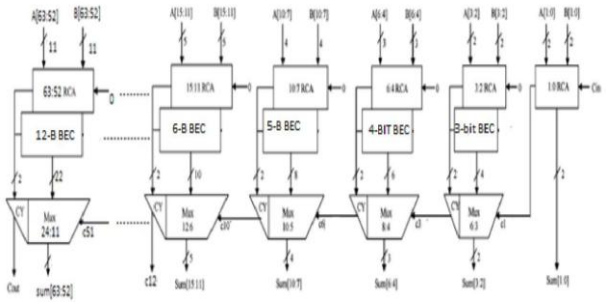

Figure-5: Modified 64-Bit SQRT CSLA

This architecture is similar to regular 64-bit SQRT CSLA, the only change is that, we replace RCA with Cin=1 among the two available RCAs in a group with a BEC. This BEC has a feature that it can perform the similar operation as that of the replaced RCA with Cin=1. Fig 5 shows the Modified block diagram of 64-bit SQRT CSLA. The number of bits required for BEC logic is 1 bit more than the RCA bits. The modified block diagram is also divided into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and corresponding MUX.

As shown in the Fig.5, Group 0 contain one RCA only which is having input of lower significant bit and carry in bit and produces result of sum[1:0] and carry out which is acting as mux selection line for the next group, similarly the procedure continues for higher groups but they includes BEC logic instead of RCA with Cin=1.Based on the consideration of delay values, the arrival time of selection input C1 of 8:3 mux is earlier than the sum of RCA and BEC. For remaining groups the selection input arrival is later than the RCA and BEC. Thus the sum1 and c1(output from mux) are depending on mux and results computed by RCA and BEC respectively. The sum2 depends on c1 and mux. For the remaining parts the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's.

Thus, the delay of the remaining MUX depends on the arrival time of mux selection input and the MUX delay. In this Modified CSLA architecture, the implementation code for Full Adder and Multiplexers of 6:3, 8:4, and 10:5 up to 24:11 were designed. The design code for the BEC was designed by using NOT, XOR and AND gates. Then 2, 3, 4, 5 up to 11-bit ripple carry adder was designed.

Word Size	Adder	Delay (ns)	Area (um^2)	Power (uW)			Power-Delay Product(10^{-15})	Area-Delay Product(10^{-25})
				Leakage Power	Switching power	Total power*		
8-bit	Regular CSLA	1.719	991	0.007	101.9	203.9	350.5	1703.5
	Modified CSLA	1.958	895	0.006	94.2	188.4	368.8	1752.4
16-bit	Regular CSLA	2.775	2272	0.017	263.7	527.5	1463.8	6304.8
	Modified CSLA	3.048	1929	0.013	235.9	471.8	1438.0	5879.6
32-bit	Regular CSLA	5.137	4783	0.036	563.6	1127.3	5790.9	24570.2
	Modified CSLA	5.482	3985	0.027	484.9	969.9	5316.9	21845.7
64-bit	Regular CSLA	9.174	9916	0.075	1212.4	2425.0	22246.9	90969.3
	Modified CSLA	9.519	8183	0.057	1025.0	2050.1	19514.9	77893.9

*Total power = leakage power + Internal power + Switching power

Table-2: Comparison of Regular CSLA and Modified SQRT CSLA

VIII. SIMULATION RESULTS

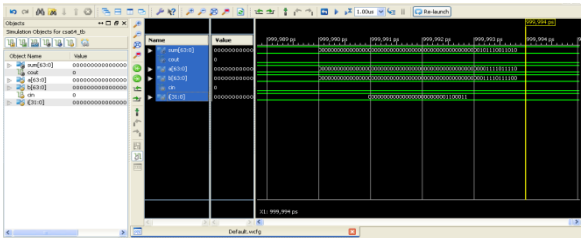

Figure-6: Regular 16-SQRT CSLA Simulation

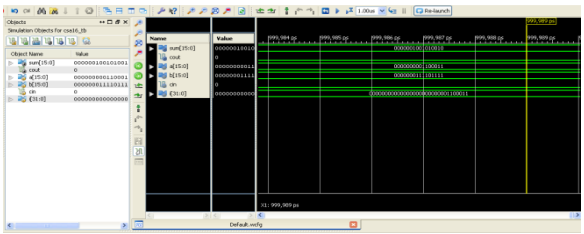

Figure-7: Modified 16-SQRT CSLA Simulation

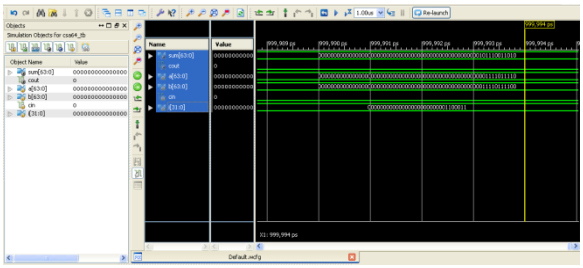

Figure-8: Modified 64-SQRT CSLA Simulation

IX. CONCLUSION

A regular CSLA uses two copies of the carry evaluation blocks, one with block carry input is zero and other one with block carry input is one. Regular CSLA suffers from the disadvantage of occupying more chip area. The modified CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-1 converter. This paper proposes a scheme which reduces the delay, area and power than regular and modified CSLA by replacing RCA with BEC.

X. FUTURE SCOPE

As our paper deals with the 64-bit CSLA there is a greater reduce in the area and power by replacing the RCA with BEC. In future, by the implementation of 128-bit we can largely reduce the area and power. By replacing BEC with D-latches which internally consists of Carry look ahead adders which is largely needed by the upcoming mobile industry.

REFERENCES

[1] O. J. Bedrij, "Carry-select adder," IRE Trans. Electron. Comput., pp. 340–344, 1962

[2] B. Ramkumarr, H. M. Kittur, and P. M. Kannan, "ASIC implementation of modified faster carry save adder," Eur. J. Sci. Res., vol. 42, no. 1, pp. 53–58, 2010.

[3] T. Y. Ceiang and M. J. Hsiao, "Carry-select adder using single ripple carry adder," Electron. Lett., vol. 34, no. 22, pp. 2101–2103, Oct. 1998.

[4] Y. Kim and L.-S. Kim, "64-bit carry-select adder with reduced area," Electron. Lett., vol. 37, no. 10, pp. 614–615, May 2001.

[5] J. M. Rabaey, Digtal Integrated Circuits—A Design Perspec- tive. Upper Saddle River, NJ: Prentice-Hall, 2001.

[6] Y. He, C. H. Chang, and J. Gu, "An area efficient 64-bit square root Carry-Select Adder for low power applications." in Proc. IEEE Int. Symp. Circuits Syst., 2005, vol. 4, pp. 4082–4085.

BIOGRAPHY

U. SANDHYA is currently pursuing B.Tech in ECE at **KITE Women's College of Professional Engineering Sciences**, Shabad, R.R Dist.

T.LAKSHMI BHAVANI is currently pursuing her B.Tech in ECE at **KITE Women's College Of Professional Engineering Sciences**, Shabad, R.R Dist.

D.Arunkumar-Graduated(B.Tech) from Vaagdevi College Of Engineering in Electronics and Communication Engineering and **Master in Engineering** from Vasavi college of Engineering in Embedded Systems and VLSI Design. Presently he is working in **KITE Womens College of Professional Engineering Sciences as a Asst. Professor**.

B.Krishna completed **B.Tech** in ECE From Dr.Paul-Raj Engineering College Bhadrachalam(JNTUH) in 2005 and ,**M.Tech**(VLSI-SD) From SITAMS-Chittoor(JNTUH) in 2008. Presently he is working in **KITE Womens College of Professional Engineering Sciences as a Asst. Professor.**